1. Lab questions

What is the difference between signed and unsigned overflow?

```
  4'b1101
+ 4'b0011
---------
 1'b1000
```

no extra carry

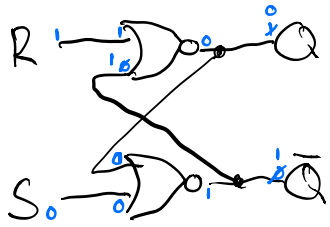
unsigned ⇒ 5 + 3 = 8

no unsigned overflow

4-bit signed ⇒ 5 + 3 = -8

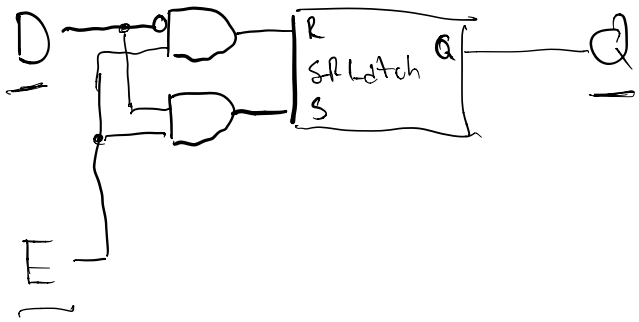
signed overflow

2. Sequential logic review

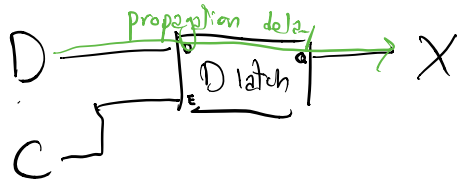


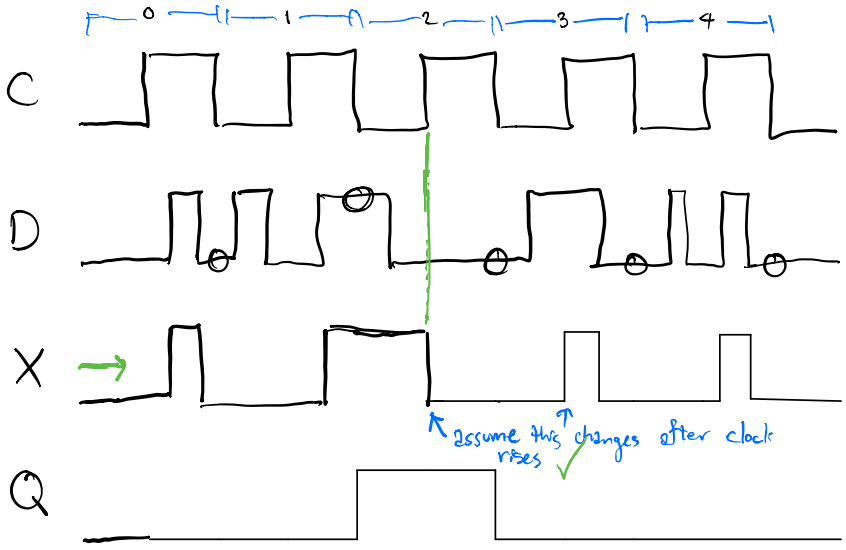
S	R	Q	$\bar{Q}$	Q_{next}	$\bar{Q}_{next}$
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
→ 0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0

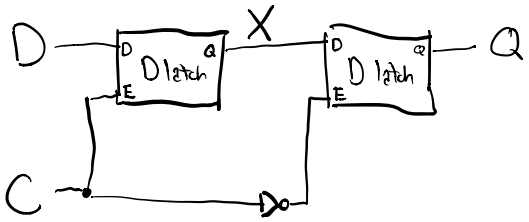
D-latch



Timing Diagram





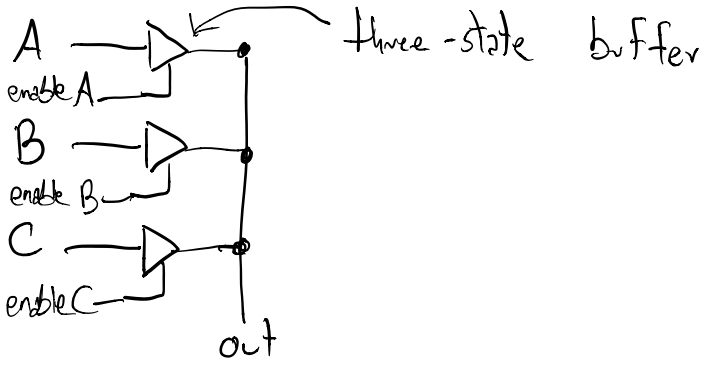


Falling-edge flip-flop

SRAM

How is SRAM different from register file?

Register files use a multiplexor w/ ~32, ~16, ... inputs
SRAM would 64K inputs to its mux., so we use a shared bit line instead.



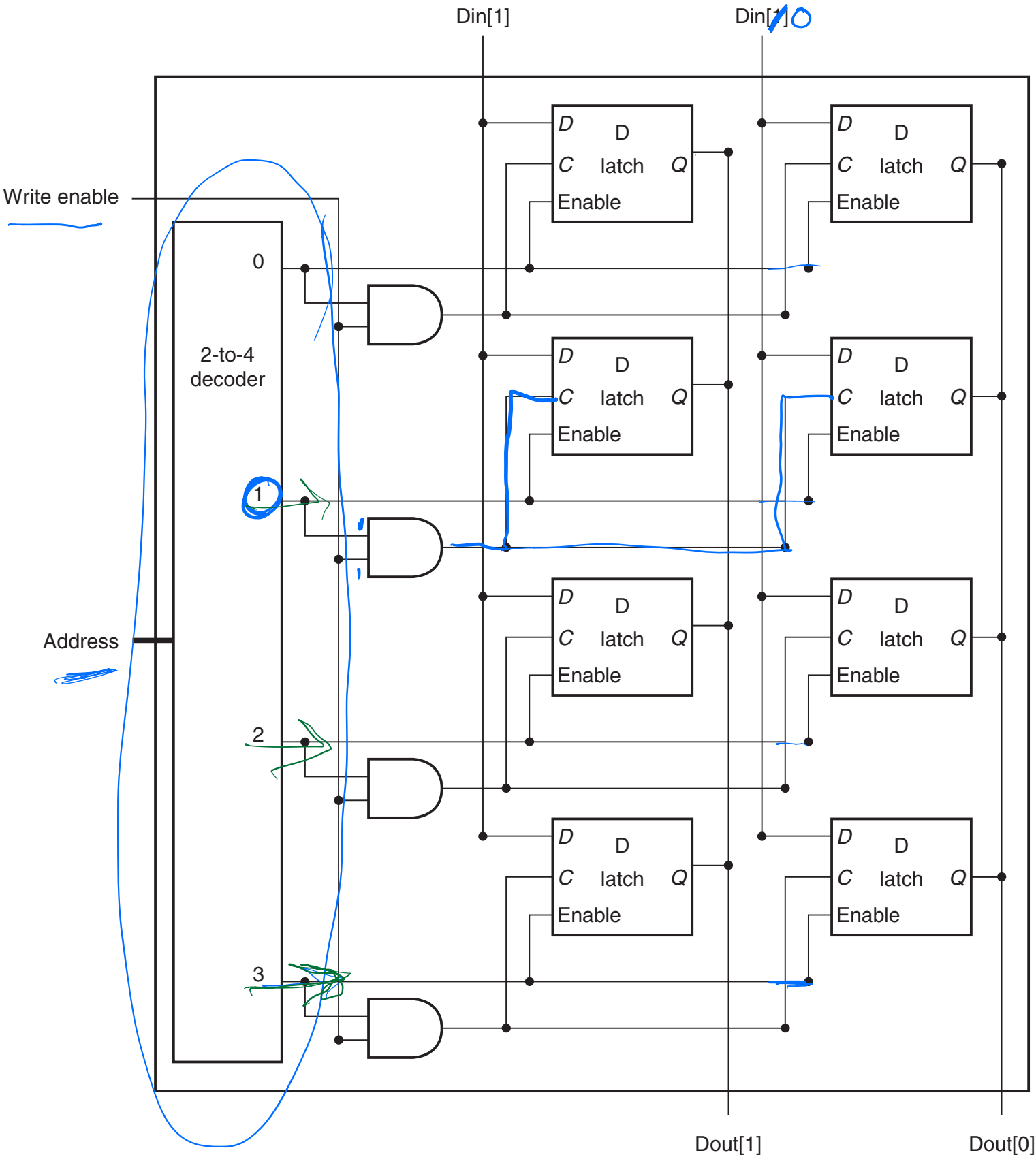
Register file: ~~array~~ table of registers (which are groups of flip-flops) that we access using an index.

SRAM: a much larger table of latches that we access using an index.

Why have both?

SRAM is good for large amounts of memory

Register files are good for a small number of values that you use and change frequently.


Din[1]
Din[0]
Write enable
Address
2-to-4
decoder
0
1
2
3
D
C
Enable
latch
Q
Dout[1]
Dout[0]

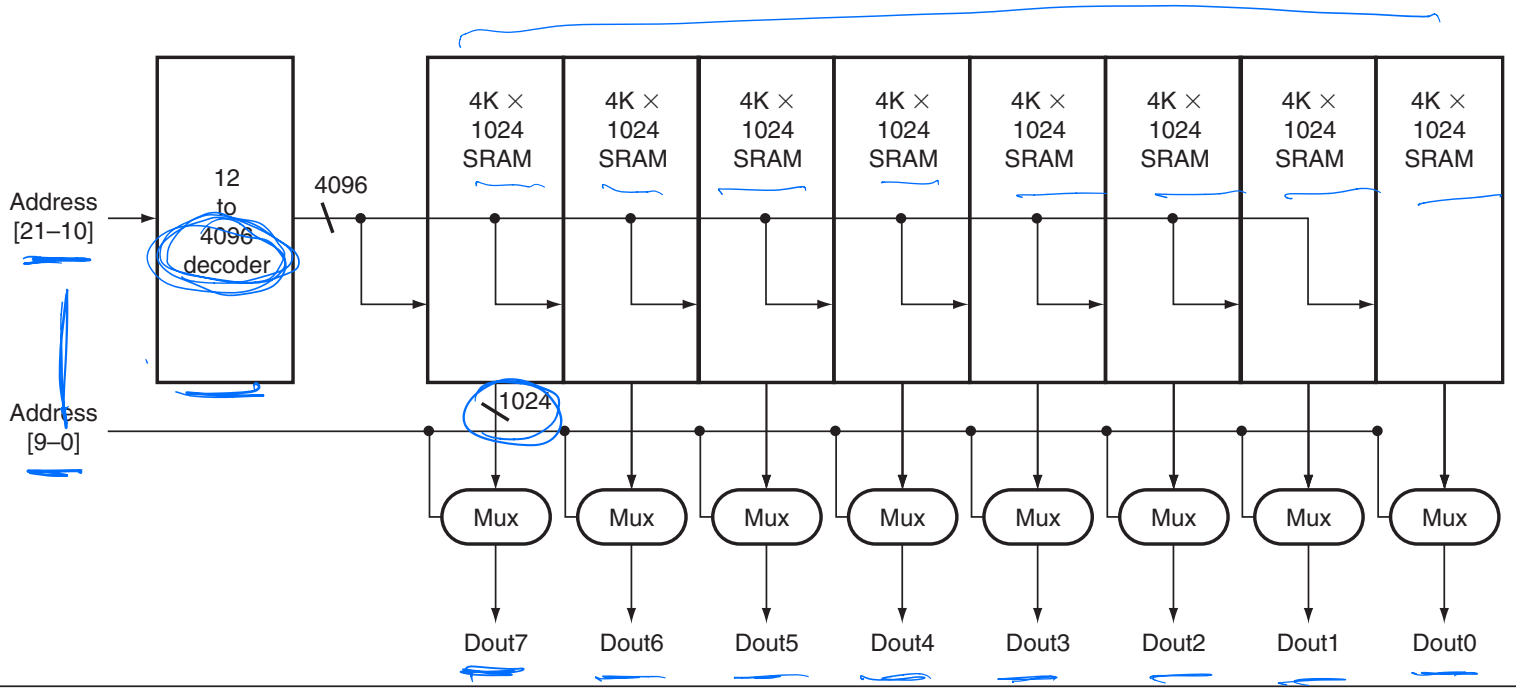


FIGURE B.9.4 Typical organization of a 4M × 8 SRAM as an array of 4K × 1024 arrays. The first decoder generates the addresses for eight 4K × 1024 arrays; then a set of multiplexors is used to select 1 bit from each 1024-bit-wide array. This is a much easier design than a single-level decode that would need either an enormous decoder or a gigantic multiplexor. In practice, a modern SRAM of this size would probably use an even larger number of blocks, each somewhat smaller.

DRAM

Less convenient than SRAM, but stores more data.

SRAM uses latches to store each bit

DRAM uses a capacitor ← small, simple
→ more storage in a small area

Complications:

① reads are destructive
after reading from DRAM, write back in

② reads are usually large
one read will access (and clear) thousands of bits even if you only need one bit.

③ values fade over time (milliseconds)
stored values must be refreshed (read and re-written)

④ capacitors can change charge when hit by cosmic rays.
some DRAM uses error-correcting codes to detect and correct errors